

Low-Power Radiation Tolerant 4GHz Bandwidth 16k Channel Spectrometer ASIC, Phase I

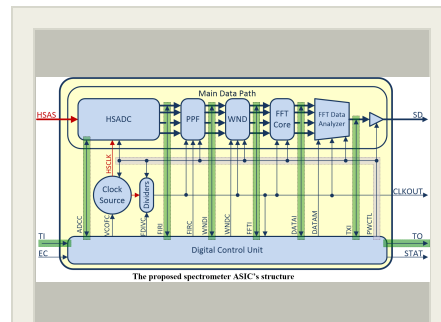
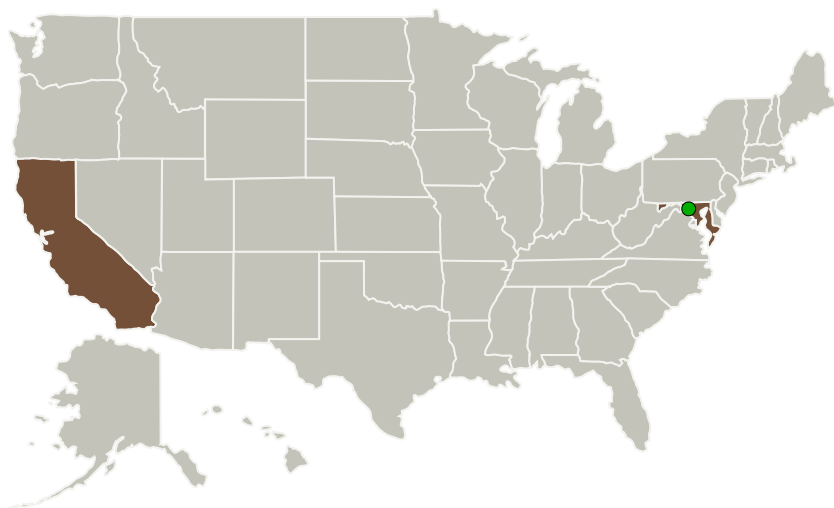
Completed Technology Project (2017 - 2017)



Project Introduction

Spectrometers currently employed or under development by NASA are based on a printed circuit board (PCB) including field programmable arrays (FPGAs) and a number of other discrete components. An application specific integrated circuit (ASIC) based spectrometer offers a great reduction in weight, volume and power consumption compared to the FPGA/PCB based implementation. This proposal aims to develop a radiation-hardened (RH) low-power (LP) poly-phase spectrometer (PPS) ASIC. The proposed RH LP PPS ASIC aims to achieve a 4GHz bandwidth and 214 (16384) frequency bins. In order to implement the required functionality and meet the specifications while consuming below 2.5W of power, the proposed ASIC will include a state-of-the-art ADC, a demultiplexer, a poly-phase filter bank, a windowing function, a fast-Fourier-transform core, a fast-Fourier-data analysis block, a data readout, a digital control unit and testing features. Tolerance to at least 4Mrads of total ionizing dose (TID) radiation and immunity to the single event effects (SEEs) will be achieved by employing radiation hardening by design, by layout, and by system techniques and also by applying an ultra-thin gate oxide technology for implementation. Low power consumption will be achieved by employing special multiplier-less-accumulators and multiplier-less-"butterflies". The power consumption will be further reduced by switching off the unused ASIC's blocks, down rating the clock frequency, eliminating unnecessary buffering and applying the 28nm CMOS technology. Phase I work will provide the proof of feasibility of implementing the proposed spectrometer ASIC. Phase II will result in the silicon proven ASIC's prototypes ready for commercialization in Phase III.

Primary U.S. Work Locations and Key Partners



Low-power Radiation Tolerant
4GHz Bandwidth 16k Channel
Spectrometer ASIC, Phase I
Briefing Chart Image

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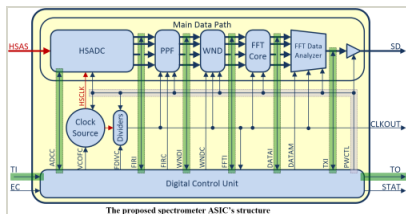


Organizations Performing Work	Role	Type	Location
Pacific Microchip Corporation	Lead Organization	Industry	Culver City, California
● Goddard Space Flight Center(GSFC)	Supporting Organization	NASA Center	Greenbelt, Maryland

Primary U.S. Work Locations

California	Maryland
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Images



Briefing Chart Image

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Briefing Chart Image
(<https://techport.nasa.gov/image/135429>)

Organizational Responsibility

Responsible Mission Directorate:

Space Technology Mission Directorate (STMD)

Lead Organization:

Pacific Microchip Corporation

Responsible Program:

Small Business Innovation Research/Small Business Tech Transfer

Project Management

Program Director:

Jason L Kessler

Program Manager:

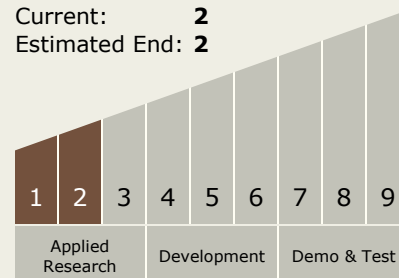
Carlos Torrez

Principal Investigator:

Aliaksandr Zhankevich

Technology Maturity (TRL)

Start: **1**
Current: **2**
Estimated End: **2**



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Technology Areas

Primary:

- TX08 Sensors and Instruments
 - └ TX08.1 Remote Sensing Instruments/Sensors
 - └ TX08.1.4 Microwave, Millimeter-, and Submillimeter-Waves